IN THE CLAIMS:

Claim 1 (Currently Amended): A method of manufacturing a semiconductor device, comprising the steps of:

forming a ~~patterned~~ tunnel oxide film, a floating gate electrode, a dielectric film, ~~and~~ a control gate electrode patterned in a cell region of a semiconductor substrate, and a gate electrode patterned in a peripheral circuit region of the semiconductor substrate;

~~forming a gate electrode in a peripheral circuit region of the semiconductor substrate;~~

removing an exposed portion of a device isolation film in the cell region by a self-align source etch process;

forming a first capping layer and a second capping layer on the semiconductor structure;

performing a self-align source annealing process for the cell region;

forming a source and drain junction in the cell region; and

forming a low concentration source and drain junction in the peripheral circuit region;

forming a gate spacer in the peripheral circuit region; and

forming a high concentration source and drain junction in the peripheral circuit region.

Claim 2 (Previously Presented): The method according to claim 1, wherein a thickness of the first capping layer is 100-200Å.

Claim 3 (Previously Presented): The method according to claim 1, wherein a thickness of the second capping layer is 50-150Å.

Claim 4 (Previously Presented): The method according to claim 1, wherein the gate spacer is formed of the first capping layer, the second capping layer, and an oxide film by a blanket etch process.

Claim 5 (Previously Presented): The method according to claim 4, wherein a thickness of the oxide film is 1200-1600Å.

Claim 6 (Currently Amended): The method according to claim 4, wherein the oxide film is etched using the second capping layer as an etch stopper and the ~~first~~ second capping layer ~~are~~ is etched through to ~~lateral portions of the second~~ the first capping layer to form a screen oxide film.

Claim 7 (Previously Presented): The method according to claim 1, wherein the source and drain junction in the cell region is formed by using the first capping layer and the second capping layer as an ion implantation screen oxide film.

Claim 8 (Previously Presented): The method according to claim 1, wherein the low concentration source and drain junction in the peripheral circuit region is formed by using the first capping layer and the second capping layer as an ion implantation screen oxide film.

Claim 9 (Previously Presented): The method according to claim 1, wherein the high concentration source and drain junction in the peripheral circuit region is formed by using a lateral portion of the first capping layer etched as an ion implantation screen oxide film.

Claim 10 (Previously Presented): The method according to claim 1, wherein the first capping and the second capping layer prohibit formation of a local bird's beak of the dielectric film formed between the floating gate electrode and the control gate electrode.